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Method and System for Self-Invalidating Self-Downgrade Cache Coherence Protocols

Type	Status	Posted	Expires
Patent	Available	04/24/2022	TBD

Description

Methods and systems for self-invalidating cachelines in a computer system having a plurality of cores.

Tech Quadrant

Technical Description

Embodiments described relate to coherence in multiprocessor systems, and, more particularly to a novel approach of enforcing coherence via data-race detection.
More specifically, a system and method is described that provides coherence by self-invalidating and writing through shared data on data-race detection points.

Description of Figure

Figure 1 depicts an exemplary multiprocessor architecture including a read-after-write race detector.
System 100 includes four cores (processors) 102 each of which have their own, private level 1 (L1) cache 104, and a share lower level cache (LLC) 106. Additionally, computer system 100 includes a read-after-write (RAW) race detector 108. The RAW race detector 108 can be implemented as a signature based table that sits at the level of the LLC 106.
Arrows 110, 112 and 114 represent various access/request messages.

Potential Commercial Uses

Used in multi-core processor systems.
Provides an efficient self-invalidation and write-through coherence system and method that guarantees the most common memory consistency models (including Total Store Order, Weak Memory Ordering and Release Consistency).
Retains valuable properties of self-invalidation protocols to include: simplicity, low cost and compatibility with virtual caches.

Figure

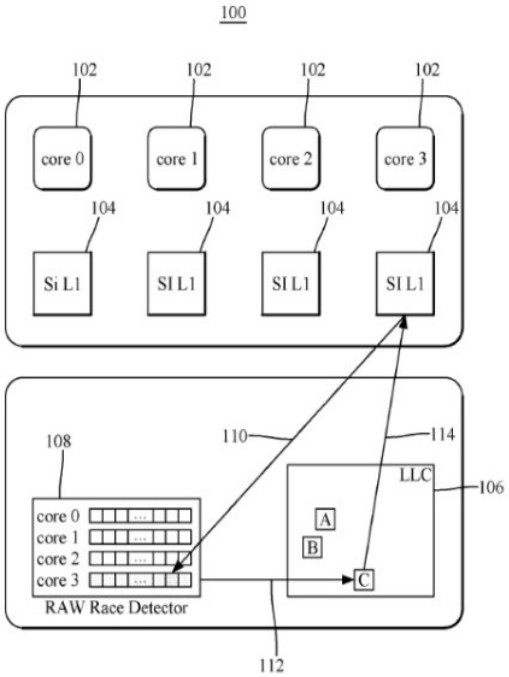

FIG. 1